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# BEAM SIGNAL PROCESSING FOR THE FERMILAB LONGITUDINAL AND TRANSVERSE BEAM DAMPING SYSTEMS


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## SUMMARY

A beam signal processor is used to secure the position of each charged bunch in the Fermilab main synchrotron. The signal processor operates at 317 MHz, 6 times the fundamental beam component and utilizes an amplitude-to-phase converter/hard limiter combination to obtain a normalized position signal. The normalization process is complete in less than 10 ns and is effective over a 23 dB intensity range. The methods used to sample and process the 2 ns beam signal are discussed and the principle parameters of the device listed. The processor outputs the derived position data to elements in a closed-loop beam damping system.


## INTRODUCTION

A "super-fast" beam position processor together with associated beam control equipments form the basis of a beam damping system which is part of the main synchrotron of the Fermilab accelerator. The beam damping system is designed to effectively reduce instabilities due to intensity related dynamical effects in the intensity range above about $5 \times 10^{12}$ protons. As an integral part of the dampers closed-loop feedback system the position processor produces a voltage proportional to the difference between the desired beam position, (the effective center of the aperture) and the actual displaced position which is a measure of the beam's controlled position. The position processor located functionally ahead of the digital storage and beam deflection electronics, thus generates the input actuating signal for the damping control servo loop.

Prior investigations of the main synchrotron beam have indicated that individual charged bunches can exhibit significant variation about the axis of the aperture at high intensity and that for effective damping the beam signal must be processed for position data on a bunch-by-bunch basis. This paper describes the beam position equipment which is used to secure the required data for the damper system and the circuits unique to this device.

The described position processor circuitry utilizes an amplitude-to-phase conversion circuit, a dual quadrature rf processor/hard limiter system, and a phase sensitive demondulator to acquire the necessary normalized position signal on a per bunch basis. The principle input signals available for the position determination are voltages derived from ultra broadbandwidth beam-line mounted stripline type electrode assemblies. The developed voltages are transferred to the processing electronics via large-diameter low loss coaxial cables. The pick-up electrode signals (two per coordinate) are voltages of pulse doublet form having a 2 ns half width at half amplitude, (HAHW) and appear at a 53 MHz rate, i.e., spaced about every 18.8 ns. The design of the electrode assembly allows the difference of the developed signals, (A-B), to be odd with respect to the apertures centerline and the sum quantity (A+B), to be an even function about the center of the aperture. Each electrode signal has an amplitude that is directly proportional to intensity and each is subject to the time modulations caused by the natural programming variations used to accommodate the changes in proton velocity during an acceleration cycle as well as variations due to longitudinal instability effects.

The intensity variational effects are prevented from influencing the developed data through normalization methods over a dynamic intensity range, $3.5 \times 10^{12}$ -to-$5 \times 10^{13}$ protons and measures to accommodate as much as ± 2 ns of input time jitter from all causes are incorporated into the overall design.

The beam signal position processor was developed in three stages of effort: (1) the design of a fast TRACK and HOLD and RF MODULATOR, (2) the development of a beam signal NORMALIZER and PHASE DEMODULATOR, and (3) the design of an output BUFFER-COMPRESSOR. A summary of the overall performance characteristics is given and an outline of the functional block diagram describing the interconnection of the circuits will be briefly discussed. The major aspects of the principle circuits will be described and performance related data will be shown.

## BEAM POSITION CHARACTERISTICS SUMMARY

Processor Type - AM/FM/AM Converter w/Normalization
Operating Position Range - ± 2 cm
Resolution - ± 1 mm
Intensity Range - $3.5 \times 10^{12}$ to $-5 \times 10^{13}$ p min.
Beam Signal Sensor - Stripline Electrodes
Beam Signal Pulse Level - 2.8 - 30 VPP
Beam Signal Pulse Width - 2 ns @ HAHW
Beam Signal Rep. Rate - ≈ 53 MHz, FM, Mod.
Allowable Input Time Jitter - ± 2 ns about Nominal
Low-Level RF Ref. Sig. - 53 MHz, 1 V P-P Sinewave FM
Position Processor Input Z - 50 Ω Nominal
Position X Intensity Output - $\frac{P \times I}{2.5 \times 10^{13}}$ V/cm; 50Ω
Normalizer Type - Dual Quad Phase Processor
Normalizer Dynamic Range - 23 dB Min.
Normalize Operating Frequency - 317 MHz
Normalized Position Output - ± 3 V/cm
Phase Demodulator - Cosine Law, Balanced Mixer
Post Detection Bandwidth - 140 MHz min., 3.5 ns RT
Output Buffer - Pulse Amp Compressor
Gain/Compression Limits - Gain = 50, Compression @±2.7V
Load Impedance - 50 Ω Nominal

## FUNCTIONAL BLOCK DIAGRAM

Figure 1 shows a functional block diagram of the position detector. The principle circuit elements are the TRACK and HOLD and MODULATOR, NORMALIZER, PULSE SYNCHRONIZER, and PHASE DETECTOR/BUFFER COMPRESSOR circuits. Two input signals designated (A) and (B) are the required beam signal pulse inputs, while two output signals, position times intensity (POS x I), center Figure 1, and a NORMALIZED OUTPUT ($E_N$), right side Figure 1, are developed on a bunch-by-bunch basis. The (POS x I) signal is obtained by differencing the tracked and held signals developed in each beam signal channel. This difference signal is sensitive to intensity as well as to position and is utilized for diagnostic and monitoring purposes. It is scaled in amplitude by the DC-to-200 MHz DIFF AMP to develop an output voltage corresponding to $\frac{P \cdot I}{2.5 \times 10^{13}} \frac{\text{Volts}}{\text{cm}}$, where (P·I) is the position intensity product.

The development of the normalized position signal requires the additional processing measures indicated


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by the blocks in the center of the figure. From Figure 1, the held amplitude levels of the (A) and (B) channel beam signals are translated in a linear fashion from pulse amplitude modulation at the 53 MHz input rate to phase modulations at a carrier of 317 MHz at the same rate by the LINEAR MOD, QUAD HYBRIDS and LIMITER components and, thereafter, retranslated to pulse amplitude modulation by a phase demodulator, ($\cos\gamma,\Pi$) block.

The output signal thus generated is normalized relative to intensity and is outputted for use via a dc-140 MHz bandwidth buffering device AMPLIFIER COMPRESSOR to the digital storage/delay system. The PULSE SYNCHRONIZER, lower left of Figure 1, serves to generate timing information for the TRACK and HOLD circuits and the RETURN-to-ZERO circuits following the 500 MHz limiters. The SYNCHRONIZER also standardizes the duration of the held beam signal data to a 15 ns limit. The 15 ns duration was selected for the hold time to: (1) allow practical bandwidths to be used for processing, (2) permit a reasonable time for acquisition and settling in devices and circuits which functionally follow the position detector, (3) allow a reasonable interval for application of beam deflection pulses to interact with the beam, and (4) ensure a sufficient number of wavelets (about 5 wavelets @ 317 MHz) for use in the normalizing scheme shown.

The choice of 317 MHz as a carrier wave was also set by, (1) achievable specifications on processing components such as the quadrature hybrid operating frequencies and bandwidths, (2) mixer and splitter coupling and isolation parameters, and (3) on the number of 317 MHz wavelets desired for practical manipulation.

It will be shown below that the measure of off-axis displacement for a given coordinate is contained in the phase difference portion of the processed signal phasors at the output of the hybrids represented by ($V_a\theta$) and ($V_b\phi$) in the block diagram and that this value, being related to the ratio of the two beam electrode signal amplitudes, can be secured by simply processing hard-limited versions of the ($V_a\theta$) and ($V_b\phi$) quantities by a suitable phase demodulator. The phase demodulators output which includes the appropriate sign of the beam displacement is buffered by broadband amplifiers. These amplifiers set the output scale factor and protect sensitive digital delay devices which receive the output signals through bipolar amplitude compressors. The sensitivity, slope of the output, for equal beam signal inputs is 3 V/cm into 50 $\Omega$, throughout a 23 dB dynamic range. The displacement range, primarily controlled by the geometry of the pick-up electrodes is ± 2 cm.

## TRACK AND HOLD AND RF MODULATOR

Figure 2 contains a simplified functional diagram of the TRACK and HOLD and RF MODULATOR circuits. The beam input signal has a nominal range from 2.2-to-30 Volts P-P, and is applied to the peak detector circuit ($D_3$, $C_2$) via a resistive splitter, one port of which is used for front panel beam-signal scope viewing, and via transformers $T_1$ and $T_2$. A small forward bias voltage is applied to the peak detector diode to improve the low-end sensitivity and dynamic range of the circuit. The transformers $T_1$ and $T_2$ aid in decoupling the peak detector circuit from power-line related noise as well as from low frequency spurious signals which could otherwise enter the sensitive bias circuit. Transform- $T_1$ and $T_2$ have a bandwidth of 500 MHz with lower cut-off frequency of ≈ 20 KC. The rather large reverse pulse levels encountered in operation makes it desirable to strip the negative-going singlet part of the beam signals. This is accomplished by $R_1$ and $D_2$. Use of transformers in this circuit are somewhat non-ideal in that measures to restore wanted dc components lost by this type of coupling and the stripping action incorporated into the coupling circuit. Components $D_1$, $R_2$, $C_1$, and $R_3$, Figure 2, are used for this purpose.

Upon receipt of a beam pulse, the charging capacitor $C_2$, is charged through diode $D_3$, the combination acting as a simple positive peak detector. The potential held by $C_2$ has negligible droop owing to the high impedance characteristics of the fet-input 200 MHz BUFFER, the reversed biased discharged diodes $D_4$, and $D_5$, and the relatively short hold interval involved. At the end of the 15 ns hold time the heavily "off" biased diodes are brought into full "on" conduction by the synchronizer developed negative-going discharge pulses, upper right Figure 2. These pulses are essentially the summed, amplified, limited, and delayed versions of the A and B input signals. The discharge pulses have a duration of 4 ns @ HAHW. The discharge path for $C_2$ is through $D_4$ and $D_5$, and occurs once per each 18.8 ns of beam input, just in time to precede the next independent beam signal pulse. The TRACK and HOLD circuit together with the timing established by the SYNCHRONIZER maintains normal levels of the held quantities throughout a time jitter range of ± 2 ns in the beam data. The stretched pulse amplitude signal resulting from these processes is applied via a 200 MHz BUFFER directly to the dc coupled port of a 1 GHz bandwidth doubly-balanced mixer configured as a linear modulator. The resultant output appears as an amplitude modulated wave, where each group of 5 carrier wavelets has an amplitude corresponding to the amplitude of a particular beam signal pulse. The carrier wave is 317 MHz, 6X the fundamental Fourier component of the beam. The 6X carrier signal is developed by a frequency multiplier so as to provide phase tracking of the signals at the modulators output with the beam fundamental.

## NORMALIZER

The NORMALIZER circuit shown in Figure 1, center, is required to automatically alter the transfer functions of the signal paths between inputs $I_A$ and $I_B$ and the 500 MHz BW limiter output, so that the output signal is made independent of the chosen input variable, the beam signals intensity. The input signal variables designated by the $I_A$ and $I_B$ quantities shown, have the implied dependency on intensity (I). Unlike other normalizers, however, which form the quantity, difference signal-to-sum signal ratio, $\left(\frac{A-B}{A+B}\right)$, of the beam electrode signals by sluggish operational, AGC, logarithmic or allied ratiometric techniques, the circuit shown operates on the fast phase modulations contained in the signal quantities, ($V_a,\theta$) and ($V_b,\phi$) indicated. The phase difference angle between the $V_a$ and $V_b$ quantities is already independent of beam intensity, because the difference is related to trigonometric arc tangent functions wherein the $\left(\frac{A}{B}\right)$ or $\left(\frac{B}{A}\right)$ ratio appears in the arguments of these quantities. Thus, when only the phase angle data is processed the normalized position results.

The amplitude components of the $V_a$ and $V_b$ signals are modulated by intensity variations and a serious error in be determination of the off-axis displacement quantity by the phase demodulator, which is sensitive to both phase and amplitude, could develop. However, this undesirable dependency is removed effectively by the hard limiters ($\not{f}$), while the desired phase difference information is preserved unaltered and transmitted to the phase demodulator for detection. The limiter devices have a bandwidth of about 500 MHz centered at 300 MHz, and are designed to phase track one another for both input signal level variations and frequency within a few electrical degrees throughout the required amplitude and frequency spectrum.

To show that the normalized beam position data is contained in the above indicated signals and that a doubly-balanced mixer configured as a phase demodulator with transfer function of the form, $E_{PD} = f\ (\mathrm{Cos}\Delta\gamma)$, contains the necessary sign and magnitude information of the displacement the circuits of Figure 3 will be investigated.

At the top of Figure 3 a quadrature hybrid coupler is represented schematically. This device and the splitter/combiners represented by the ($\Sigma$) symbol (center), form the amplitude-to-phase difference conversions needed for NORMALIZER operation. The hybrid device consists of a collection of ferrite-core transformers, delay lines, and lumped $R^S$ and $C^S$. Applied signals are split into two components as indicated by the arrows and recombined after passing through the internal quadrature networks as follows:

Let $(2)^{-\frac{1}{2}}$ times the peak input quantity ($E_1$) and ($E_4$) be directly coupled to ports 2 and 3 respectively while $(2)^{-\frac{1}{2}}$ times these quantities be cross coupled in lagging quadrature form to ports 3 and 2 respectively. By representing the input signals as:

$$E_1 = A\ (\mathrm{Cos}\theta + j\ \mathrm{Sin}\theta) \qquad (1.$$

$$\text{and} \quad E_4 = B\ (\mathrm{Cos}\phi + j\ \mathrm{Sin}\phi) \qquad (2.$$

the output signals ($V_2$) and ($V_3$) appearing in matched loads at ports 2 and 3, become:

$$V_2 = K(A\ \mathrm{Cos}\theta + B\ \mathrm{Sin}\phi) + j(A\ \mathrm{Sin}\theta - B\ \mathrm{Cos}\phi) \qquad (3.$$

$$\text{and} \quad V_3 = K(A\ \mathrm{Sin}\theta + B\ \mathrm{Cos}\phi) + j(B\ \mathrm{Sin}\phi - A\ \mathrm{Cos}\theta) \qquad (4.$$

where $K = (2)^{-\frac{1}{2}}$

These signals represent the complex input-to-output transfer functions which are basic to this type of circuit element.

The summing device, center of Figure 3, adds the input ($E_x$) and ($E_y$) signals to form a single output quantity, ($V_R$). Thus, for $E_x = E_1$ and $E_y = E_4$ as above, the summed output is:

$$V_R = K\ \{(A\ \mathrm{Cos}\theta + B\ \mathrm{Cos}\phi) + j(A\ \mathrm{Sin}\theta + B\ \mathrm{Sin}\phi)\} \qquad (5.$$

where $K = (2)^{-\frac{1}{2}}$

With these basic relationships the output signals of the simple processor shown in the center of Figure 3 can be obtained as follows: the ($V_R$) signal is the same as that given in equation (5. while the port 3 signal ($V_3$), is obtained by the quadrature summing of components from port 1 and 4 to give:

$$V_3 = K\ \{(A\ \mathrm{Sin}\theta + B\ \mathrm{Cos}\phi) + j(B\ \mathrm{Sin}\phi - A\ \mathrm{Cos}\theta)\} \qquad (6.$$

The difference angle ($\Delta\gamma$), between these two signals can be obtained by forming the ratio of the imaginary to real components of each output signal dividing by B, and then differencing their respective arc tangents as follows:

$$(\Delta\gamma) = \text{arc tan}\left\{\frac{\frac{A}{B}\ \mathrm{Sin}\theta + \mathrm{Sin}\phi}{\frac{A}{B}\ \mathrm{Cos}\theta + \mathrm{Cos}\phi}\right\} - \text{arc tan}\left\{\frac{-\frac{A}{B}\ \mathrm{Cos}\theta + \mathrm{Sin}\phi}{\frac{A}{B}\ \mathrm{Sin}\theta + \mathrm{Cos}\phi}\right\} \qquad (7.$$

For the practical case where the input signals are matched in phase, $\theta = \phi$, and referring the inputs to a reference phase angle of 0 rad., the resultant difference is:

$$(\Delta\gamma) = \text{arc tan}\left(-\frac{A}{B}\right)\ \text{rad.} \qquad (8.$$

Equation (8. shows that the measure of off-axis displacement inherent in the $\left(\frac{A}{B}\right)$ ratio of the electrode voltages can be obtained by measuring ($\Delta\gamma$). Since the intensity parameter (I), Figure 1, is contained in each beam signal quantity, this factor cancels in the arguments of (7. and (8.

The derivative of (8, with respect to $\left(\frac{A}{B}\right)$ gives the sensitivity of the process, thus:

$$\frac{d}{d\left[\frac{A}{B}\right]}\ \text{arc tan}\ (\Delta\gamma) = \frac{-1}{1+\left[\frac{A}{B}\right]^2}\ \text{rad;} \qquad (9.$$

and for $\frac{A}{B} = 1$, the case which represents beam at the center of the aperture:

$$\frac{d}{d\left[\frac{A}{B}\right]} = -\tfrac{1}{2}\ \text{rad.} = \frac{-\ 3.3\ \text{Electrical Degrees}}{\text{dB Diff between A \& B}} \qquad (10.$$

The output developed by this simple processor although satisfactorily indicating the conversion principles involved suffers from two principle drawbacks which prevent efficient use of this kind of circuit in the dampers control system. Firstly, the sensitivity of 3.3°/dB is relatively low, in fact it is only about 1.5 times as large as the measured phase uncertainty error chargeable to the best obtainable limiter devices. This low sensitivity limits system position accuracy to about .67 dB or ± 8%. Secondly, and equally significant, is that equation (8. shows that a $\left(\frac{\pi}{4}\ \text{rad.}\right)$ phase difference is obtained when $\left(\frac{A}{B}\right) = 1$. This means that the device operates with a phase offset which would require phase equalization before either sine or cosine law phase demodulators could successfully process the information for an odd relation about a desired zero volt crossover corresponding to equal input signals. An added delay of $\left(\frac{\pi}{4}\ \text{rad.}\right)$ in either signal path could solve this problem but not without serious implications. Since added delays force the insertion phase shift versus frequency to be different in each channel, large Phase errors develop making this processing circuit useful only for narrow-bandwidth applications.

In contrast, two matched quadrature hybrids can be interconnected with two matched splitters to form an improved processor, Figure 3, lower. In this arrangement the two hybrids are driven from splitters so that port 4 of the lower hybrid is driven in antiphase relationship with respect to the other three inputs. When this is done, the phasors representing the ($V_a$) and ($V_b$) outputs rotate in opposite directions such that the difference angle ($\Delta\gamma$) between $V_a$ and $V_b$, with $E_A = E_1$ and $E_B = E_4$ as before, and for $\phi = 0$ rad., becomes:

$$(\Delta\Psi) \doteq \text{arc tan} \left\{\tan\theta + \frac{B}{A}\text{Sec}\,\theta\right\} - \text{arc tan} \left\{\tan\theta - \frac{B}{A}\text{Sec}\,\theta\right\} \text{ rad.} \quad (11.$$

When the phase angles of the input signals are equal as is the usual case, this function reduces to $(\Delta\Psi) = \text{arc tan}\left(\frac{B}{A}\right) - \text{arc tan}\left(\frac{-B}{A}\text{ rad.}\right)$. Note that for the case $(A = B)$ $(\Delta\Psi) = \frac{\Pi}{2}$; $(\Delta\Psi)$ increases above and below this value as the ratio $\left(\frac{B}{A}\right)$ changes above and below 1. The quadrature relationship obtained when A = B, is independent of frequency as well as for changes in the phase of the input signals, and is the basis for the direct processing of the signals by a cosine-law phase demodulator without the necessity to add equalization devices in either channel. Decade bandwidths can be obtained with this method. Since the angle varies about a $\left(\frac{\Pi}{2}\right)$ reference angle, the cosine demodulators output contains the appropriate sign of the displacement.

The sensitivity of the dual quadrature processing technique can be obtained by differentiating (11. for the condition that $\left(\frac{A}{B}\right) = 1$:

$$\frac{(d\Psi)}{d\left[\frac{A}{B}\right]} = 1 \text{ rad. or } 6.5 \text{ Electrical Degrees/dB}$$

$$\text{or} \quad = 19.5 \text{ Electrical Degrees/cm Displacement.} \quad (12.$$

This sensitivity represents a factor of two improvement over the simple processor discussed above.

The expressions developed above are based on steady-state conditions but the components in the processor have full bandwidths approaching 500 MHz, which permit these relations to hold for the modulated signals considered. The total processing time necessary to secure a normalized signal is less than 10 ns.

## PHASE DEMODULATOR, BUFFER COMPRESSOR

The phase demodulator consists of two centertapped broadband transformers coupled by a diode ring containing four matched hot-carrier diodes. The diode ring and transformer secondaries are interconnected to permit the developed load currents to be equal & opposite, on the average, when the transformer primaries are excited in quadrature with equal amplitude signals. For any relative phasing of the excitation signals, the load current is proportional to the peak signal level ($V_p$), the detectors transfer constant (K), and the cosine of the relative phase angle difference ($\Delta\Psi$). The output signal $E_{PD}$ of Figure 1, using the values associated with the devices used is:

$$E_{PD} = K\,V_p\,\text{Cos}\,(\Delta\Psi) = .147\,\text{Cos}\,(\Delta\Psi) \quad (13.$$

Using (11. to define ($\Delta\Psi$) in (13., and taking the derivitive of (13. for the condition that $\left(\frac{A}{B}\right) \leftrightarrow 1$ cm off-axis, the sensitivity of the demodulators output is:

$$E'_{PD} = .060 \text{ Volts/cm Displacement.} \quad (14.$$

The AMPLIFIER COMPRESSOR, Figure 1, has a gain of 34 dB, x 50, formed by a dc-200 MHz preamplifier stage and a dc-150 MHz x 4 power stage. The combined bandwidth is dc-140 MHz with sharp roll-off above 250 MHz to provide filtering of the second harmonic spurious developed by the phase demodulator. The response is below 46 dB above 500 MHz. An optional dc/ac coupling network allows the lower corner of the overall amplifier circuit to be made adjustable from dc to about 2 KC. The compressor portion of the device consists of three diode-resistor arrays connected in the feed-forward part of a broadband operational amplifier circuit. The compressor is designed to "soft limit" at ± 2.7 peak. The load impedance is 50 ohms.

Taking into account the amplifier compressors gain the normalized output signal ($E_N$), Figure 1, becomes:

$$E_N = E'_{PD}\,(50) = 3 \text{ Volts/cm.} \quad (15.$$

## PERFORMANCE

The performance data for the beam signal processor is shown in the oscilloscope photographs of Figures 4, 5, and 6. The photographs show the normalized output voltage developed for an input pulse doublet 2 ns HAHW, with 53 MHz rep. rate, 16 V P-P, and with ≈ .5 ns jitter. The number of pulses (bunches) in the batches is restricted so as to show typical performance when the spaces between batches is small (≈ 50 ns.). Figure 4 shows the normalized output versus the electrode voltage ratio $\left(\frac{A}{B}\right)$. Note that a ratio $\left(\frac{A}{B}\right) = 1.12$, 1 dB, is easily observed. The linearity to $\left(\frac{A}{B}\right) = 1.4$, 3 dB, ≈ 1 cm displacement, is within 5 % of best-straight-line fitting. Figure 5 indicates the normalizers performance for two $\left(\frac{A}{B}\right)$ ratios, 2 dB, and 6 dB. The data indicates little change in the normalized values when the (intensity) input signal was reduced from 0 dB, top of sequences, to -20 dB, lowest traces of sequences. Output signal change is less than 5% over the 0-20 dB range shown. Figure 6 is also presented as a means indicating overall processing speed and normalization capability. In this photograph the normalized output signal is shown for the condition that alternate bunches, following the 1st and before the last, were arranged with whole or fractional $\left(\frac{A}{B}\right)$ ratios, i.e., $\left(\frac{A}{B}\right) = 2$ or $\left(\frac{A}{B}\right) = \frac{1}{2}$, alternately. The photograph shows the alternating 15 ns pulses corresponding to this input. Note that three intensity values 0, 10, and 20 dB, corresponding to the range $2.5 \times 10^{12}$-to-$2.5 \times 10^{13}$ p. are shown and that the output remains insensitive to these changes and that the alternations are preserved in the data.

## CONCLUSION

A high-speed processor has been constructed to furnish beam position data to a beam damper system operating in the Fermilab's main synchrotron. The device determines the beam position on a bunch-by-bunch basis by processing electrode signals of 2 ns width that appear at a 53 MHz rate. The position data is normalized by a method which uses AM-to-PM-to-AM conversions, making data available on a normalized basis in less than 10 ns over an intensity range of at least 14:1. The output signal drives a 50 ohm load to ±2.7V peak where soft compression circuits protect sensitive digital equipments which functionally follow the detector in the dampers feedback chain. The position processor has been integrated into the Fermilab's main accelerator and have been operational since the latt part of 1974.

## ACKNOWLEDGEMENTS

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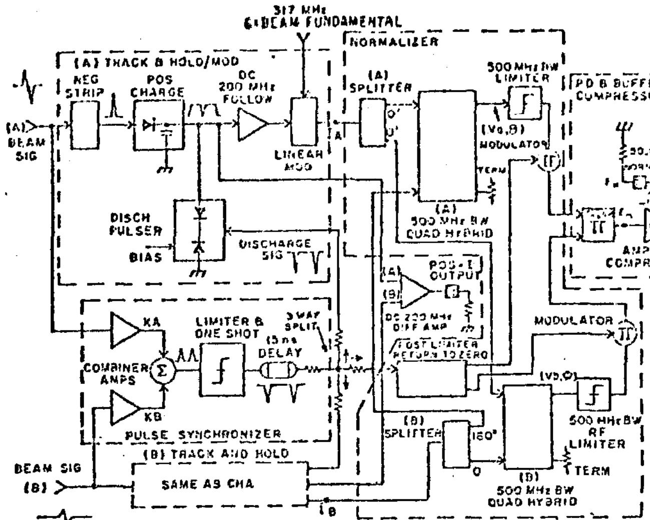
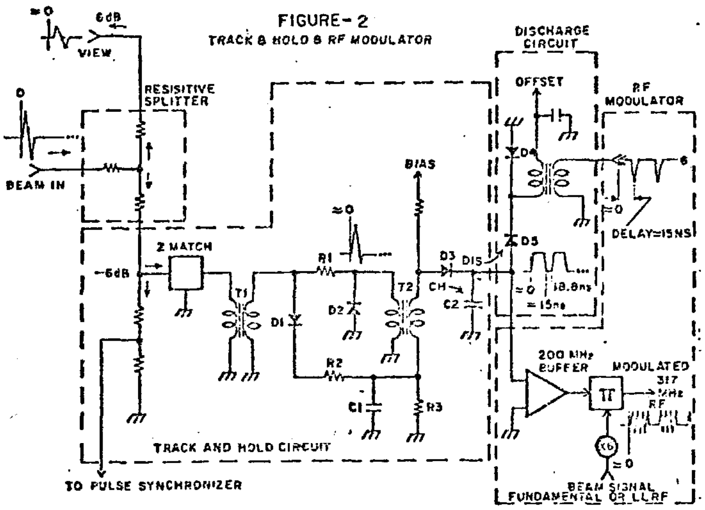



FIGURE-1 SUPERDAMPER BEAM SIG POSITION PROCESSOR

FIGURE-2

TRACK & HOLD & RF MODULATOR



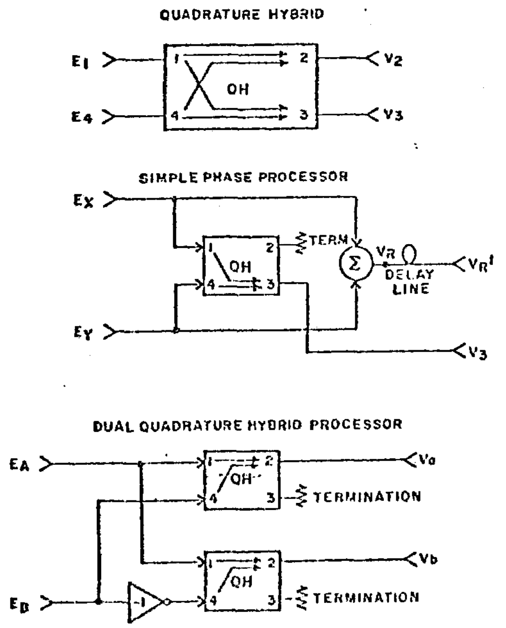




FIGURE-3

Quad Hybrid and Processor Configurations

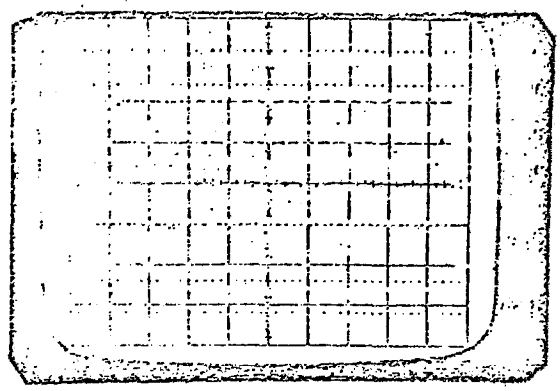


Fig. 4. Normalized Output Signal vs $\left(\frac{A}{B}\right)$ ratio in dB 50 ns/div., 26 Bunches Shown

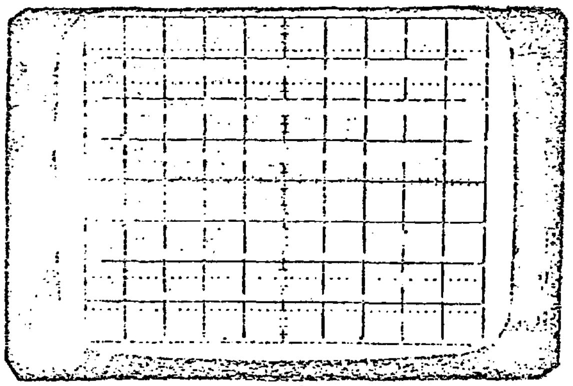


Fig. 5. Normalized Output Signal vs $\left(\frac{A}{B}\right)$ = 2 dB; Top, 6 dB, Bottom, vs Intensity 0-to-20 dB 50 ns/div., 26 Bunches Shown

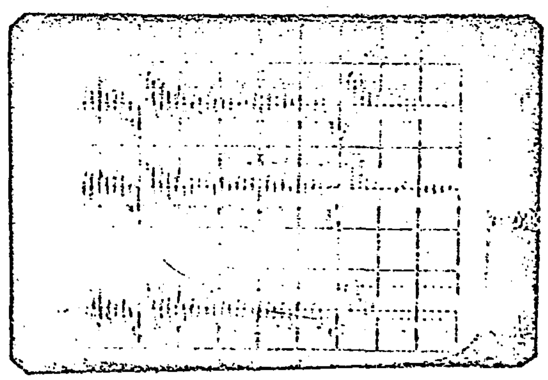


Fig. 6. Normalized Output Signal vs $\left(\frac{A}{B}\right)$ = 2; ½ Alternately, vs Intensity, 0-10-20 dB., 49 Bunches Shown